

IT IS CLAIMED:

- 1 1. In a non-volatile memory device having a plurality of memory cells to be
2 sensed in parallel, each memory cell having a source electrode, and the plurality of
3 memory cells having their source electrodes tied together into a combined source line, a
4 method of sensing comprising:
 - 5 (a) providing a predetermined demarcation current value to discriminate
6 between two memory states;
 - 7 (b) sensing the plurality of memory cells in parallel;
 - 8 (c) identifying those memory cells having conduction currents higher than
9 said predetermined demarcation current value;
 - 10 (d) inhibiting the conduction currents of those higher current memory cells
11 after identifying all those higher current memory cells among said plurality of
12 memory cells being sensed in parallel;
 - 13 (e) repeating (b) to (d) for a predetermined number of times; and
14 (f) sensing the plurality of memory cells in parallel in a final pass.
- 1 2. The method of claim 1, wherein said predetermined number of times is
2 zero.
- 1 3. The method of claim 1, wherein said predetermined number of times is
2 one or greater.
- 1 4. The method of claim 1, wherein:
2 the conduction currents of said plurality of memory cells are sensed
3 though a plurality of associated bit lines; and
4 said step of identifying those high current memory cells includes:
5 precharging said plurality of associated bit lines with a constant current
6 source having a predetermined current limitation;
7 identifying those memory cells having conduction currents higher than
8 said predetermined demarcation current value by their associated bit lines'
9 precharging rates.
- 1 5. The method of claim 1, wherein:

2 said sensing is performed by an associated plurality of sense amplifier in
3 parallel; and
4 said step of identifying those high current memory cells includes:
5 identifying those memory cells by using their associated sense
6 amplifiers to compare their conduction currents relative to said
7 predetermined demarcation current value.

1 6. The method of claim 1, wherein:
2 the conduction currents of said plurality of memory cells are sensed
3 though a plurality of associated bit lines; and
4 said inhibiting the conduction currents includes pulling the associated bit
5 lines of those memory cells to ground.

1 7. The method of claim 1, wherein:
2 said plurality of memory cells is non-volatile memory.

1 8. The method of claim 1, wherein:
2 said plurality of memory cells is flash EEPROM.

1 9. The method as in any one of claims 1-8, wherein:
2 each memory cell stores one bit of data.

1 10. The method as in any one of claims 1-8, wherein:
2 each memory cells stores more than one bit of data.

1 11. In a non-volatile memory device having a plurality of memory cells to be
2 sensed in parallel, each memory cell having a source electrode, and the plurality of
3 memory cells having their source electrodes tied together into a combined source line, a
4 read system comprising:
5 a controller; and
6 a plurality of sensing circuits for sensing said plurality of memory cells in
7 parallel, each sensing circuit further comprising:

8 a discriminator coupled to receive a conduction current of an
9 associated memory cell, said discriminator discriminating whether the
10 conduction current is higher or lower than a predetermined demarcation
11 current value;
12 a latch being set to register the associated memory cell in response
13 to said discriminator identifying a conduction current higher than said
14 predetermined demarcation current value;
15 an inhibitor to turn off the conduction current of the associated
16 memory cell;
17 an inhibitor enabler responsive to said plurality of sensing circuits
18 having their discriminators completed their identifications and said latch
19 being set; and wherein
20 said controller controls said plurality of sensing circuits to operate
21 a predetermined number of times before reading out the determined
22 memory state.

1 12. The read circuit as in claim 11, wherein said predetermined number of
2 times is two.

1 13. The read circuit as in claim 11, wherein said predetermined number of
2 times is greater than two.

1 14. The read circuit as in claim 11, further comprising:
2 a precharge circuit which is a constant current source having a
3 predetermined current limitation; and wherein:
4 the conduction currents of said plurality of memory cells are sensed
5 through a plurality of associated bit lines;
6 said precharge circuit precharging said plurality of associated bit lines; and
7 said plurality of sensing circuits identifying those memory cells having
8 conduction currents higher than said predetermined demarcation current value by
9 their associated bit lines' precharging rates.

1 15. The read circuit as in claim 11, wherein:

2 said plurality of sensing circuits identifying those memory cells having
3 conduction currents by comparing their conduction currents relative to said
4 predetermined demarcation current value.

1 16. The read circuit as in claim 11, wherein:
2 the conduction currents of said plurality of memory cells are sensed
3 though a plurality of associated bit lines; and
4 said inhibitor turns off the conduction currents by pulling the associated
5 bit lines of those memory cells to ground.

1 17. The read circuit as in claim 11, wherein:
2 said plurality of memory cells is non-volatile memory.

1 18. The read circuit as in claim 11, wherein:
2 said plurality of memory cells is flash EEPROM.

1 19. The read circuit as in any one of claims 11-18, wherein:
2 each memory cell stores one bit of data.

1 20. The read circuit as in any one of claims 11-18, wherein:
2 each memory cell stores more than one bit of data.

1 21. In a non-volatile memory device having a plurality of memory cells to be
2 sensed in parallel, each memory cell having a source electrode, and the plurality of
3 memory cells having their source electrodes tied together into a combined source line, a
4 read system comprising:
5 a controlling means; and
6 a plurality of sensing circuits for sensing conduction currents of said
7 plurality of memory cells in parallel, each sensing circuit further comprising:
8 means for discriminating whether the conduction current is higher or lower
9 than a predetermined demarcation current value;

10 means for registering the associated memory cell in response whenever its
11 conduction current is identified to be higher than said predetermined demarcation
12 current value;
13 inhibitor means for inhibiting the conduction current of the associated
14 memory cell;
15 means for enabling said inhibitor means responsive to said
16 plurality of sensing circuits having their discriminators completed their
17 identifications and said latch being set; and wherein
18
19 and
20 means for inhibiting the associated memory cell with said higher
21 conduction current; and wherein
22 said controlling means operating said plurality of sensing circuits a
23 predetermined number of times before reading out the sensed memory state in a
24 final pass.

1 22. The read circuit as in claim 21, wherein said predetermined number of
2 times is two.

1 23. The read circuit as in claim 21, wherein said predetermined number of
2 times is greater than two.

1 24. The read circuit as in claim 21, further comprising:
2 a precharge circuit which is a constant current source having a
3 predetermined current limitation; and wherein:
4 the conduction currents of said plurality of memory cells are sensed
5 through a plurality of associated bit lines;
6 said precharge circuit precharging said plurality of associated bit lines; and
7 said plurality of sensing circuits identifying those memory cells having
8 conduction currents higher than said predetermined demarcation current value by
9 their associated bit lines' precharging rates.

1 25. The read circuit as in claim 21, wherein:

2 said plurality of sensing circuits identifying those memory cells having
3 conduction currents by comparing their conduction currents relative to said
4 predetermined demarcation current value.

1 26. The read circuit as in claim 21, wherein:
2 the conduction currents of said plurality of memory cells are sensed
3 though a plurality of associated bit lines; and
4 said inhibitor means turns off the conduction currents by pulling the
5 associated bit lines of those memory cells to ground.

1 27. The read circuit as in claim 21, wherein:
2 said plurality of memory cells is non-volatile memory.

1 28. The read circuit as in claim 21, wherein:
2 said plurality of memory cells is flash EEPROM.

1 29. The read circuit as in any one of claims 21-28, wherein:
2 each memory cell stores one bit of data.

1 30. The read circuit as in any one of claims 21-28, wherein:
2 each memory cell stores more than one bit of data.

1 31. A non-volatile memory, comprising:
2 an array of memory storage units;
3 a plurality of sense amplifiers for sensing a group of memory storage units in
4 parallel;
5 each of said plurality of sense amplifiers having predetermined properties
6 dependent on a set common parameters and a set of control signals; and
7 a reference circuit sharing a common environment with said plurality of sense
8 amplifier, said reference circuit for calibrating said set of common parameters with
9 respect to the common environment and generating said set of control signals accordingly
10 so that said plurality of sense amplifiers are controlled to have its predetermined
11 properties enforced.